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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/520,314	01/05/2005	Joost Maarten Zitzmann	NL 020593	2573

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EXAMINER	
LIN, PHYOWAI	
ART UNIT	PAPER NUMBER
2613	

MAIL DATE	DELIVERY MODE
08/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/520,314	ZITZMANN ET AL.	
	Examiner	Art Unit	
	PHYOWAI LIN	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/05/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The references listed in the Information Disclosure Statement filed on January 05,2005 have been considered by the examiner (see attached PTO-1449 form).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1 and 2** are rejected under 35 U.S.C. 102(e) as being anticipated by Imajo (US Pub Number 2002/0122233).

Regarding to claim 1, Imajo discloses an optical receiver circuit (see FIG.9) comprising:

an optical converter circuit (38) (light receiving circuit with a light receiving diode 10) converting optical power into electrical power (see paragraph [0111], lines 1-5 and FIG.9);

a sensor circuit detecting a characteristic value of the electrical power (see paragraph [0018], lines 1-5 where in from point B to CPU 24 functioning like sensor circuit part which can detect the value of the electrical power (received light voltage value);

an attenuator circuit (44) (electronic attenuator 22) having a variable attenuation, the attenuation being controlled by the characteristic value of the electrical power output by the sensor circuit so as to obtain a constant output signal level of the optical receiver circuit (see paragraph [0113],lines 1-3; paragraph [0111],lines 6-14 and FIG.9).

Regarding to claim 2, Imajo disclose everything claimed as applied above (see claim 1). In addition, the optical receiver circuit further includes: wherein the optical converter (38) comprises a photodiode (light receiving diode 10) (see paragraph [0111], lines 1-5 and FIG.9).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Imajo (US Pub Number 2002/0122233) in view of Farmer et al. (US Pub Number 2004/0253003).

Regarding to claim 3, Imajo disclose everything claimed as applied above (see claim 1). In addition, the optical receiver circuit further includes: wherein the sensor circuit comprises a resistor network (58, 60) (resistor 11) connected to the optical converter circuit (38) in order to derive a control voltage V.sub.CONTR as the characteristic value of the electrical power output by the optical converter circuit (38) (see paragraph [0118], lines 1-5; paragraph [0111], lines 6-10 and FIG.9 where in a resistor 11 connects in series with light receiving diode 10 and from point B derives a received light voltage value and then the received light voltage value couples to CPU 24 in order to derive output control voltage).

Even though Imajo discloses a receiving circuit having resistor 11 connects in series with light receiving diode 10, he fails to specially disclose another resistor from resistor network (58,60), which connects to the light receiving diode 10.

Farmer et al. in the same field of endeavor, disclose optical receiving circuit having resistor network (58,60) (resistor network as 340,410), which connects to the light receiving diode 117 (see paragraph [0089], lines 14-22 and FIG. 4).

Therefore, it would have been obvious to a person of ordinary skill in the art at the same time the invention was made to modify Imajo's invention as to use decoupling resistor 410 (part of resistor network 58,60) in optical receiving circuit because it would allow the optical receiving circuit having decoupling resistor 410 for preventing modulated current flow into the gain controller (control voltage)).

7. **Claims 4,6,7 and 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Imajo (US Pub Number 2002/0122233) in view of Weigand (US Patent Number 6489856).

Regarding to claim 4,Imajo disclose everything claimed as applied above (see claim 1). However, he fails to explicitly disclose that electronic attenuator 22 which use step attenuation type and having plurality of cascaded attenuator stages.

Weigand disclose wherein the attenuator circuit (44) is a step attenuator circuit (step attenuation circuit 15b-see FIG.2) comprising a plurality of cascaded attenuator stages which can be selectively switched to active states (see column 4,lines 4-49 and FIG.2 where in step attenuation circuit 15b, 22, 15a are formed in cascaded attenuator stages and based on bit control signal 14 and 16 is turned on to logic high, it can turn the step attenuator circuits 15b, 22, 15a to active state).

Therefore, it would have been obvious to a person of ordinary skill in the art at the same time the invention was made to modify Imajo's invention as to use step attenuator circuit type and the circuits are cascaded because it would allow the attenuation will be arithmetically additive provided return loss of each unit is extremely good in optical receiving circuit.

Regarding to claim 6,Imajo and Weigand disclose everything claimed as applied above (see claim 4). In addition, Weigand disclose the optical receiving circuit further includes: wherein the respective attenuator stages each have a different attenuation value (see column 4,lines 4-49 and FIG.2 where in any appropriate resistance value can change the attenuation level of step attenuator circuits15b, 22, 15a so that each step attenuator circuit can have a different attenuation value).

Therefore, it would have been obvious to a person of ordinary skill in the art at the same time the invention was made to modify Imajo's invention as to use plurality of step attenuator circuits each have a different attenuation value because it would allow the optical receiver circuit having desire output optical output power level based on different attenuation value.

Regarding to claims 7and 10,Imajo and Weigand disclose everything claimed as applied above (see claim 1). In addition, Weigand disclose the optical receiving circuit further includes: wherein the attenuator stages are attenuator stages comprising a resistor (resistor R3) and a semiconductor switch (FET Q3) in series with the resistor and where in semiconductor switch is MOFET (FET Q3) (see column 3, lines 58-62 and FIG.2).

Therefore, it would have been obvious to a person of ordinary skill in the art at the same time the invention was made to modify Imajo's invention as to use step attenuator circuit with particular resistor and transistor values because it would allow the optical receiver circuit having desire output optical output power level based on variable step attenuation circuit.

8. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Imajo (US Pub Number 2002/0122233).

Regarding to claim 5,Imajo and Weigand disclose everything claimed as applied above (see claim 4). In addition, Imajo discloses the optical receiver circuit in FIG.9 having two A/D converters before and after the CPU circuit for converting the control voltage signal from digital state to analog state. But only one A/D converter is required by the applicant's invention for converting the control voltage signal from analog state to digital state.

However, it is well known in the art that using A/D converter circuit can switch electrical signal level from either digital state to analog state or analog state to digital state based on design choice.

Therefore, it would have been an obviousness to combine the well known in the art with Imajo invention as using only one A/D converter circuit after the CPU for digitizing the output control voltage to control the attenuation stage of the optical receiving circuit because it would allow the optical receiving circuit having reliable, accurate output power signal.

9. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Imajo (US Pub Number 2002/0122233) in view of Kasashima et al. (US Patent Number 5694069).

Regarding to claim 8,Imajo discloses everything claimed as applied above (see claim 1). However, he fails to specifically disclose in the optical receiving circuit having two resistors and one semiconductor switch in series and one of the resistors being bridged by another semiconductor switch.

Kasashima et al. disclose in the optical receiving circuit having two resistors (resistors 13,14) and one semiconductor switch (switch 11) in series and one of the resistors being bridged by another semiconductor switch (switch 12) (see FIG.1 where in two resistors 13 and 14 are connected with FET switch 11 in series and one of the resistor 14 is being bridged by another FET switch 12).

Therefore, it would have been obvious to a person of ordinary skill in the art at the same time the invention was made to modify Imajo's invention as to use two resistors with one semiconductor switch in series and one of the resistor is being bridged to another semiconductor switch in optical receiving circuit because it would allow the optical receiving circuit having low power consumption and high switching states by using semiconductor FET switch.

Allowable Subject Matter

10. **Claim 9** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Citation of Pertinent Prior Art

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Inamori et al. disclose cellular mobile telephone terminal having receiving circuit with control section for controlling the attenuation level of receiving circuit.

Otaka disclose attenuation circuit using gate current control of FET conduction to vary attenuation for making better electrical circuit.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHYOWAI LIN whose telephone number is (571) 270-1659. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PWL 08/22/07

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KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER